Claims

1. An FET comprising:

a gate having a top and bottom portion, the top portion having a width that is greater than the width of the bottom portion; and

a diffusion self-aligned to the bottom portion.

2. The FET as recited in claim 1, wherein said diffusion comprises a first implant.

3. The FET as recited in claim 2, wherein said first implant comprises a halo implant.

4. The FET as recited in claim 2, wherein said first implant is directed at an angle from the normal to provide said implant self-aligned to said bottom portion.

5. The FET as recited in claim 1, further comprising a second implant defined by said top portion.

6. The FET as recited in claim 5, wherein said second implant comprises an extension implant.

7. The FET as recited in claim 1, further comprising a spacer adjacent said top portion and a third implant defined by said spacer.

8. The FET as recited in claim 7, wherein said third implant comprises a source/drain implant.

9. An FET comprising a gate, said gate comprising first conductive material and a second conductive material different from said first conductive material, said second conductive material on said first conductive material, wherein said second conductive material extends beyond said first conductive material to provide a T-shaped gate.

10. The FET of claim 9, wherein said first conductive material is on a gate dielectric and said gate dielectric is on a substrate.

11. The FET of claim 9, wherein said first material has a dimension less than a photolithographic minimum dimension.

12. The FET of claim 9, wherein said first material comprises a first semiconductor material.

13. The FET of claim 12, wherein said first semiconductor material comprises germanium.

14. The FET of claim 12, wherein said first semiconductor material comprises a germanium compound Ge_xSi_{1-x}, wherein x is in the range of about 0.5 to about 1.0.

15. The FET of claim 9, wherein said second conductive material comprises polysilicon.

16. The FET of claim 9, wherein said first conductive material comprises polysilicon.

17. The FET of claim 16, wherein said second conductive material comprises a refractory metal.

18. The FET of claim 17, wherein said second conductive material comprises tungsten, tantalum, molybdenum, or titanium.

19. The FET of claim 9, wherein said second conductive material comprises a silicide.

20. The FET of claim 9, further comprising a spacer along sidewalls of said second conductive material.

21. The FET of claim 13, wherein an air gap is left behind said spacer along a notched sidewall of said first conductive material.

22. A method of fabricating a semiconductor device comprising the steps of:

providing a substrate formed of a first material, said substrate having a surface;

forming a gate dielectric on said surface;

forming a gate conductor on said gate dielectric;

chemically reacting edges of said gate conductor adjacent said gate dielectric to form a first reaction product; and

selectively removing said first reaction product with respect to remaining portions of said gate conductor so as to provide a notch in said gate conductor.

23. The method as recited in claim 22, wherein the step of forming a gate conductor comprises a first gate layer and a second gate layer, wherein said first gate layer contacts said gate dielectric and said second gate layer is on said first gate layer.

24. The method as recited in claim 23, wherein the step of chemically reacting edges of said first gate layer forms said first reaction product.

25. The method as recited in claim 24, wherein the step of selectively removing said first reaction product further includes removing said first reaction product with respect to remaining portions of said first gate layer and said second gate layer so as to provide a notch in said first gate layer.

26. The method as recited in claim 22, further comprising providing a spacer along sidewalls of said second gate layer.

27. The method as recited in claim 26, wherein an air gap is left behind said spacer along sidewalls of said first gate layer.

28. The method as recited in claim 22, wherein said first gate layer comprises germanium.

29. The method as recited in claim 22, wherein said first gate layer comprises a germanium compound Ge_xSi_{1-x}, wherein x is in the range of about 0.5 to about 1.0.

30. The method as recited in claim 22, wherein said second gate layer comprises silicon.

31. The method as recited in claim 22, wherein in said first reaction product comprises germanium oxide, or silicon germanium oxide.

32. The method as recited in claim 22, wherein said first gate layer comprises silicon.

33. The method as recited in claim 32, wherein said second gate layer comprises a refractory metal.

34. The method as recited in claim 33, wherein said second gate layer comprises tungsten, tantalum, or titanium.

35. The method as recited in claim 33, wherein said second gate layer comprises a silicide.

36. The method as recited in claim 22, wherein said first reaction product comprises silicon dioxide.

37. The method as recited in claim 22, wherein said first reaction product comprises a silicide.

38. The method as recited in claim 22, wherein said second gate layer comprises a silicide.

39. The method as recited in claim 22, further comprising the steps of

providing metal along sidewalls of said gate conductor; and

recess etching said metal.

40. The method as recited in claim 39, wherein the step of chemically reacting further includes the step of:

reacting said gate conductor with said metal to form a silicide along edges of said gate conductor adjacent said gate dielectric.

41. The method of claim 40, wherein the step of selectively removing said first reaction product further includes:

etching away said silicide.

42. The method of claim 40, wherein said silicide formed along edges of said gate conductor adjacent said gate dielectric is cobalt silicide, or titanium silicide.

43. The method of claim 42, wherein the step of selectively removing said cobalt silicide or said titanium silicide includes using an hydrogen peroxide mixture, or a hot sulfuric/hydrogen peroxide mixture.

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